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Technical Note

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A Gridded Thick Film Metalization Structure Employed in Multichip Circuit Fabrication

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Lincoln Laboratory
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Lexington, Massachusetts

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LINCOLN LABORATORY

A GRIDDED THICK FILM METALIZATION STRUCTURE EMPLOYED IN MULTICHIP CIRCUIT FABRICATION

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Group 87

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ABSTRACT

This technical note describes a process to produce a thick film circuit that holds as many as 40 integrated circuit chips and can be produced quickly at reasonable cost. Yield, equipment, materials and circuits are also listed.

Accepted for the Air Force
James W. Malley
Acting Project Officer

Gridded Thick Film For Multichip Circuits Saves Time, Costs

A way to make a 1 inch square, gridded thick film circuit that holds as many as 40 integrated circuit chips, and can be produced quickly at reasonable cost, has been developed.

Key to the process was development of a basic circuit board that has reduced the time and cost of producing custom layouts for individual circuit designers. The board consists of a gold ground plane, 39 gold bottom lines, insulation, and 22 gold top lines that provide 858 crossovers and 907 openings to the bottom conductor for wire bonding. This network is screened and fired onto a 1 x 1 x 0.025-inch, 96 percent alumina substrate.

For the array circuits, dielectric pads with gold metalization are screened onto the board. Chips mounted on the metalized pads are interconnected by wire bonding as well as by cuts in the top and bottom conductor lines. The complete integrated array can be mounted in a 72-lead package and hermetically sealed.

Producing the Board

The basic board, drawn 20X (Fig. 1) final size, is placed on a digitizer (Calma, Model 485) to transfer coordinate information to magnetic tape. This information, processed via an IBM 360 computer, is transferred to a punched paper tape that is fed into an IBM 2250 display scope to visually display the board to detect errors or to make changes. The tape is then fed through a David Mann pattern generator to produce a 1:1 photographic plate of the pattern for screen fabrication. This procedure was repeated three times to make screens for the top and bottom lines and insulation layer.

Azacol "R" direct emulsion was applied to a 6 x 6 inch stainless steel screen, which was held in contact with the photographic plate and exposed by

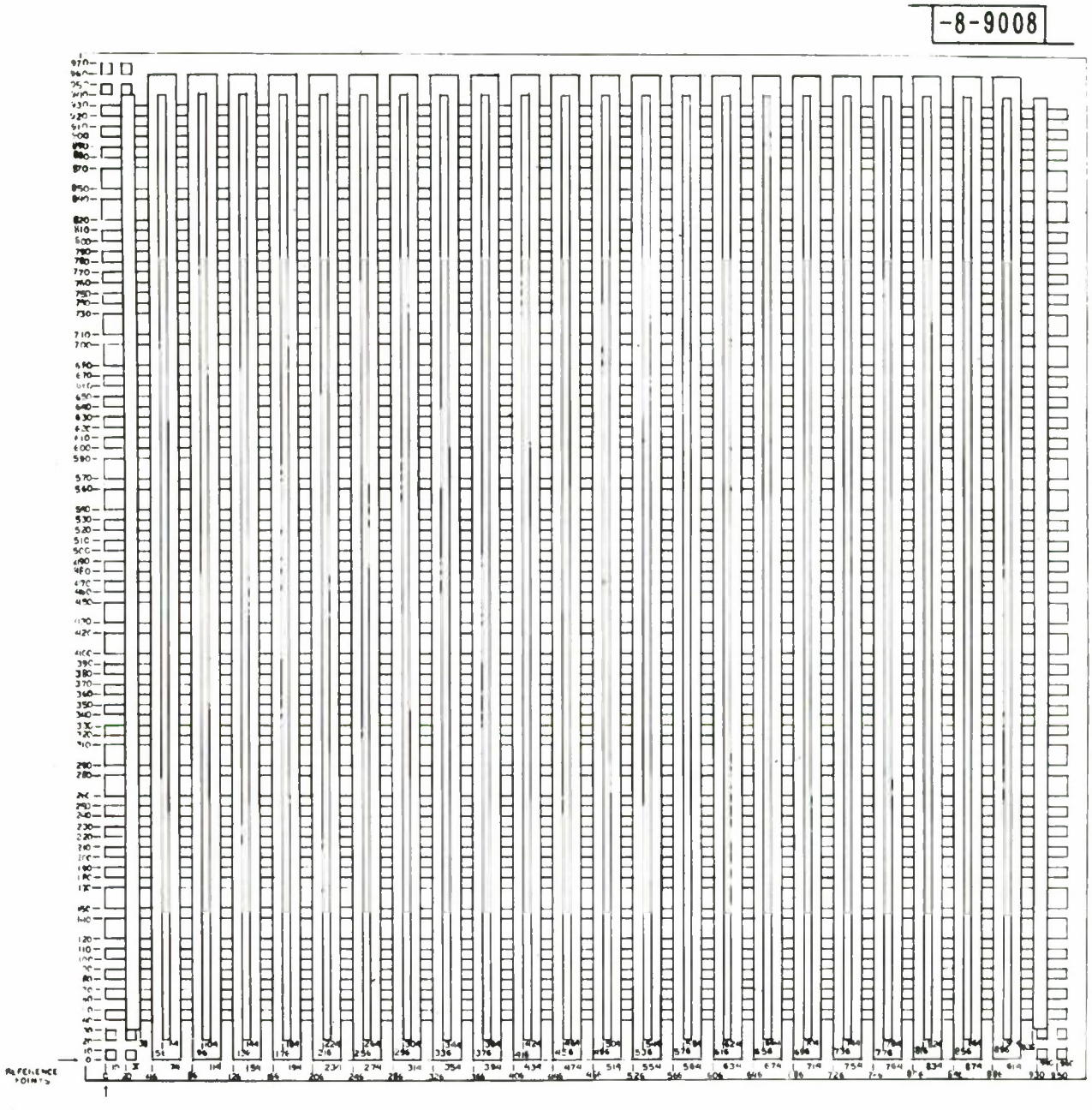

Fig. 1. Drawing of basic board.

a 4 inch, mercury arc, collimated light for approximately one minute per mil of emulsion thickness. Underexposure produced a "washed out" emulsion; overexposure decreased line widths and produced a sawtooth appearance. The direct emulsion was found more durable than indirect emulsions; and by careful processing, lines as narrow as 0.005 inch were printed consistently. The final emulsion was 0.0025 to 0.003 inch thick.

Screen tensions were monitored by applying a one pound force to the screen and the deflection was measured in thousandths of an inch with a Presco Model STG-3 screen tension gauge. Normal deflections were 35-55 mils for a 200 mesh screen, 40-60 mils for a 250 mesh screen.

All printing was done "off contact," i.e., a gap of 0.035 to 0.040 inch separated the substrate and screen. The gap was made by bringing the substrate in contact with the screen and then backing off the carriage via its height adjustment until the desired separation is read on the dial indicator. The carriage is then locked in place and the screen aligned to the substrate.

The squeegee was centered over the substrate and lowered to the screening position. With a light shining from the back, squeegee height was adjusted by micrometer screws until no space was visible between the substrate and screen. A 1-3/4 inch long, polyurethane (60 Durometer) squeegee, slightly rounded at the edges to minimize screen damage, and that does not overlap the substrate by more than 1/2 inch on each side, has been found most effective.

Processing

To apply the 0.990 x 0.990 inch ground plane to the back side of the substrate a solderable, high adhesion gold paste with a viscosity of 180,000 centipoise (cp) was squeegeed through a 200 mesh (0.0016) direct emulsion screen. The large area and high viscosity required two squeegee strokes to obtain a uniform layer.

After screening, the gold paste was slumped for five minutes and then predried for 10 minutes at 125°C in a forced air, stainless steel oven. The substrate was fired for 12 minutes at 1000°C peak in the conductor furnace. On cooling, it was inspected visually and checked for thickness, conductivity, solderability and adhesion to the substrate.

The bottom conductor lines were applied to the other side of the substrate. A dense (high metal-to-glass ratio) gold paste with high conductivity and viscosity of 348,000 cp was pushed through a 200 mesh (0.0016) direct emulsion screen. The lines produced were excessively thick (0.0009 inch) resulting in separations down the middle of the 0.020 wide lines (Fig. 2).

Splitting of the lines was overcome by lowering the viscosity of the gold paste to 240,000 cp and using a 250 mesh, direct emulsion screen. The slump time was 10 minutes, predry at 100°C was another 10 minutes, and firing in the conductor furnace followed this 57 minute profile.

Rise time: 55°C/min.

Soak time: 11 min. at 940°C.

Cooling time: 36°C/min.

The firing cycle was used for all the other firings to produce the basic board and its circuit arrays.

The 0.0005 inch thick, dense-fired, conductor lines had a conductivity of 0.0063 ohms/square. A 0.001 inch gold wire was attached by thermocompression bonding to the bottom conductor lines at various places to check adhesion to the substrate. In all cases, the wire broke before the gold separated from the substrate.

The glass ceramic insulator has a low dielectric constant (K = 8-12), and when fired at high temperature (900°- 1000°C) crystallizes and will not remelt during subsequent firings, reducing drastically the possibility of pinholes -- the major cause of shorts between conductive layers.

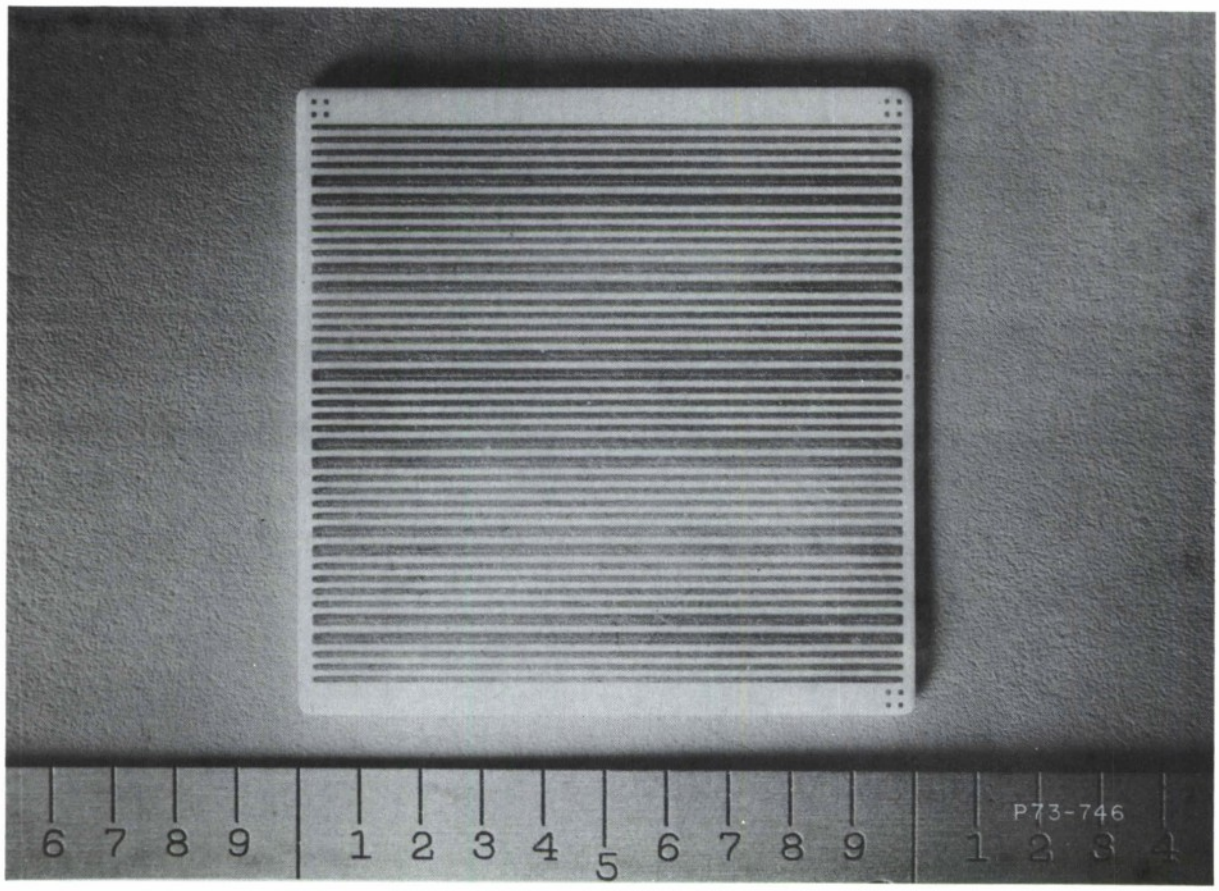

Fig. 2. Bottom conductor lines; 0.010-inch wide with 0.010-inch spacing, every fifth and sixth line 0.020-inch wide with 0.010-inch spacing.

Three methods of applying the dielectric were tried, but only one was found satisfactory.

1. A 165 mesh screen with a direct emulsion and paste viscosity of 280,000 cp produced sharp edges and little or no flow during screening, but surface cracks developed after firing. Thickness was 0.0014 inch.
2. A 200 mesh (0.0016) screen with a direct emulsion and paste viscosity of 140,000 cp was used to screen, fire, rescreen, and refire. A usable 0.0016 inch thick dielectric with no cracking or pinholes was produced.
3. A 200 mesh (0.0016) screen with a direct emulsion and a paste viscosity of 140,000 cp was used to screen, slump for 10 minutes, and dry for 10 minutes at 100°C. A second layer was applied after cooldown. Not slumped, but dried for 10 minutes at 100°C, the spreading between insulators was roughly 10-20 percent, maintaining 0.006 to 0.008 inch open space after firing.

The third method was preferred because it required one less step than method 2 while providing a fairly smooth dielectric film which was free of pinholes and cracks. The final fired thickness was 0.0022 inch for the two layers (Fig. 3).

The paste comprising the bottom conductors was screened through a 250 mesh, direct emulsion screen to form the top conductors. These 0.0005 to 0.0006 inch thick top conductor lines (Fig. 4) had a conductivity of 0.0074 ohms/square. Adhesion was tested in the same way the bottom conductors were checked, and with similar results.

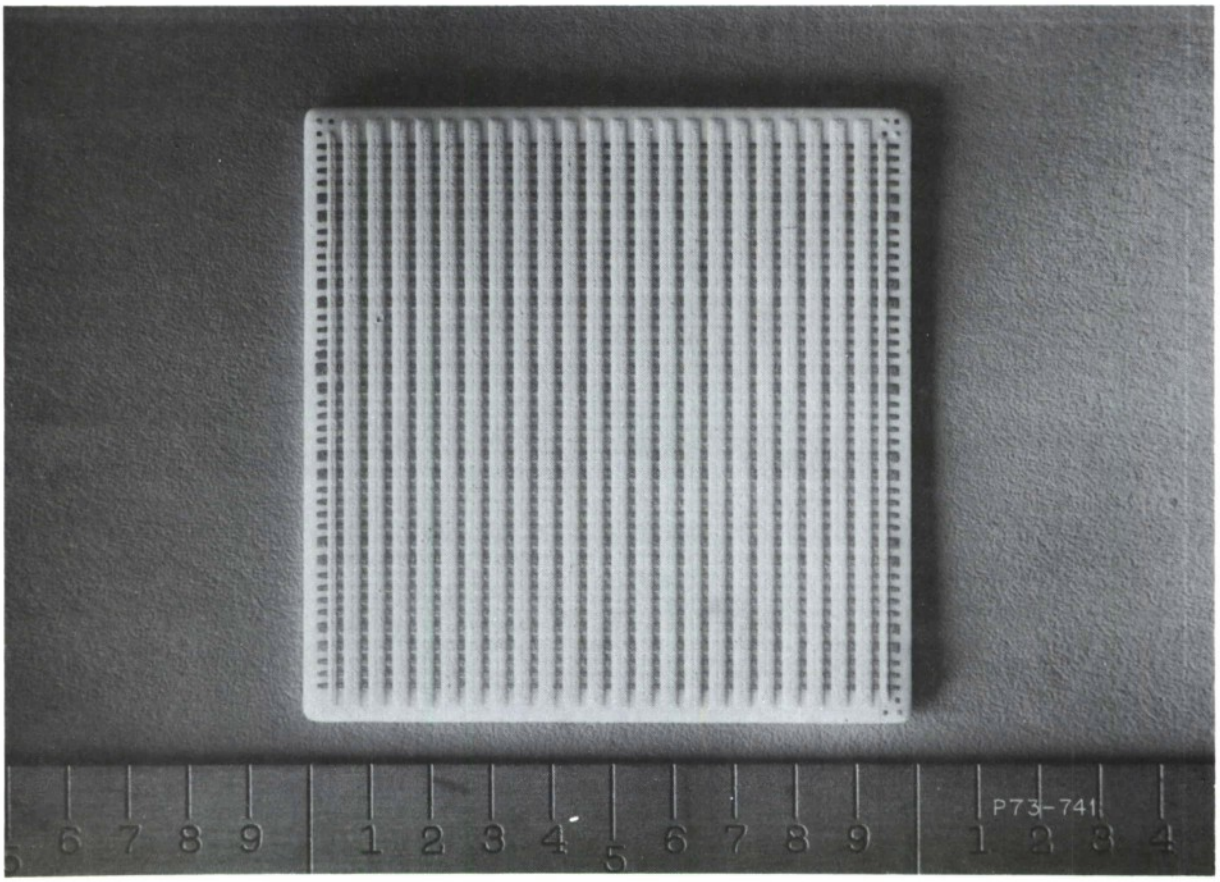

Fig. 3. Dielectric lines.

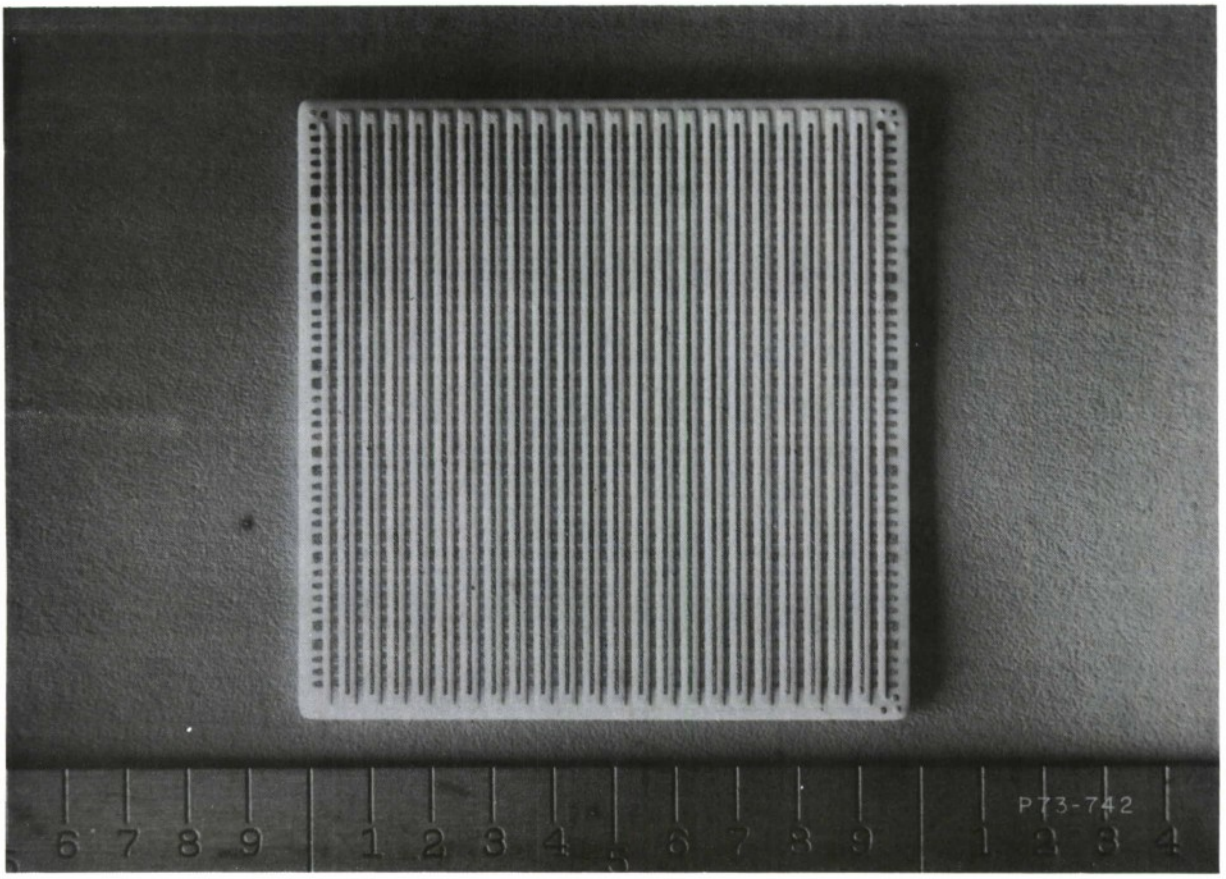

Fig. 4. Top conductor lines; 0.008-inch wide.

Visual inspection revealed some "open" lines caused by a hair or lint during screening, especially in the 0.008 inch wide top conductor lines.

Electrical continuity of the lines was checked. A check for electrical short circuits between conductor layers with a 100 V DC megohmmeter indicated their resistance was greater than 2×10^{12} ohm. Capacity between the 0.008 inch wide top lines and 0.010 inch wide bottom lines was 0.5 to 1.0 pf, and the capacity between the 0.008 inch top lines and 0.020 inch bottom lines was 0.8 to 1.6 pf. Dissipation factors were less than one percent. Theoretically, these values should be lower.

Twenty of the 240 substrates that passed electrical and mechanical inspection were subjected to three thermal cycles from -50 to 125°C suffered no visual or electrical changes. Twenty substrates and three thermal cycles were felt sufficient testing for this application.

Chip Pad Fabrication

Working from a schematic drawing of an array of integrated circuit chips, the necessary pads, cuts and wire bonds for the chips were drawn on a copy of the basic board (Fig. 5). Processed through the digitizer, IBM 360 and David Mann pattern generator in the same manner as the basic board, three masks were made with which to build the pads on the board to mount the integrated circuit array.

The same glass ceramic insulator material used on the basic board was laid down as fill material between dielectric lines -- and the same height as the dielectric lines -- via a 165 mesh, direct emulsion screen. The paste, whose viscosity was 280,000 cp, was slumped for five minutes, dried for 10 minutes at 100°C, and fired.

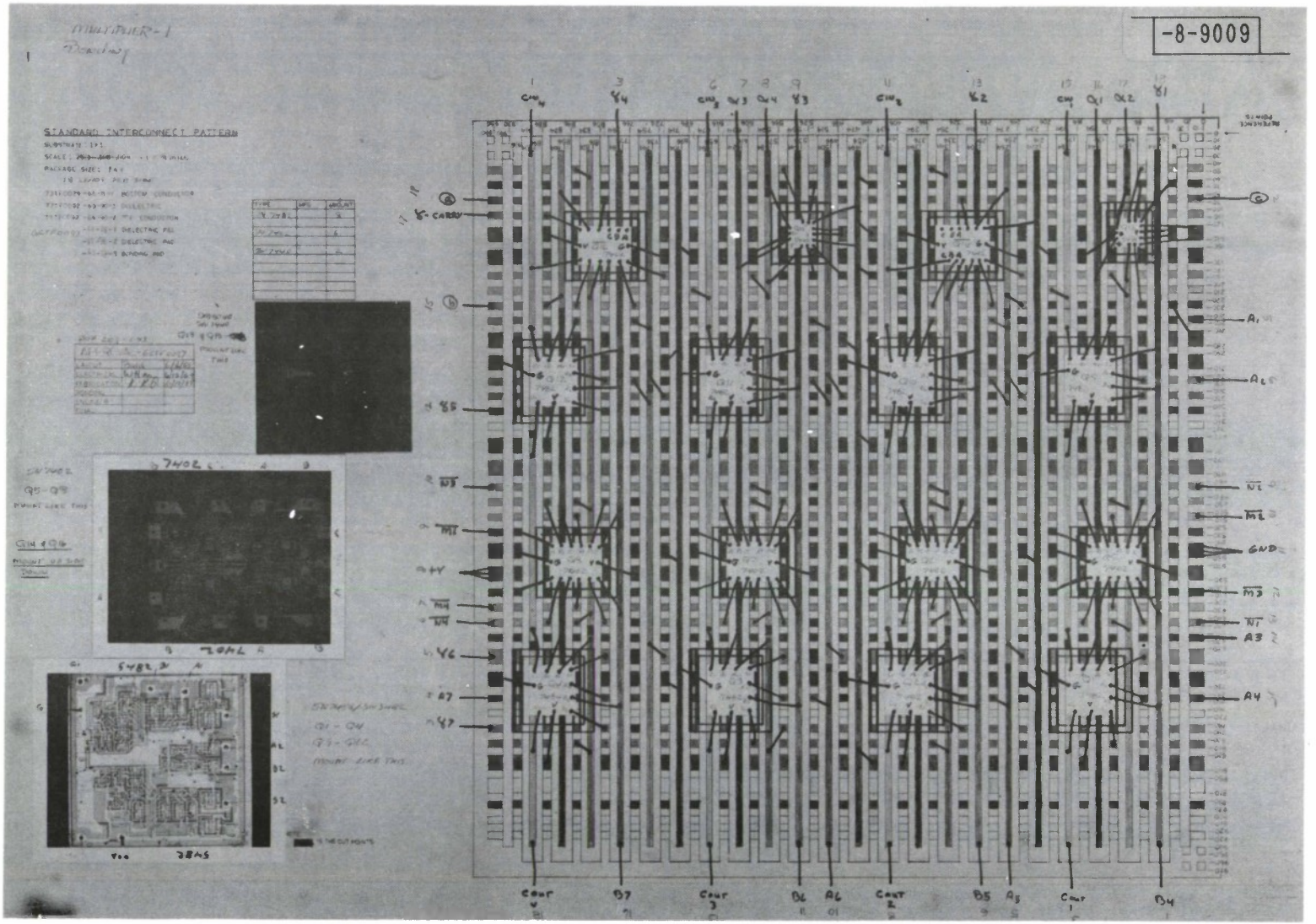

Fig. 5. Assembly drawing of an integrated array.

The same glass ceramic dielectric, but with a viscosity of 140,000 cp, formed the dielectric pad via a 200 mesh (.0016) direct emulsion screen. The pads were slumped for five minutes, dried for 10 minutes at 100°C and fired. The pads (Fig. 6) were inspected for cracks and smoothness.

A solderable, high adhesion, gold paste with viscosity of 180,000 cp was laid down via a 200 mesh (.0016) direct emulsion screen to form the metallized chip pad. The gold paste was slumped for five minutes, dried for 10 minutes at 125°C, and fired. The adhesion was tested, the thickness checked, and the existence of cracks determined.

Cuts were made in the top and bottom conductors using an air abrasive resistor trimmer. A 0.007 inch nozzle provided a 0.009-0.011 inch cut (Fig. 7). The substrates were cleaned ultrasonically in trichlorethylene, dried in a vacuum oven at 100°C for 30 minutes and given a complete visual and electrical inspection.

The integrated circuit chips were mounted by two different methods. Originally, it was by silver epoxy; later, using a gold-silicon preform the chips were bonded eutectically at 390°C.

After the chips were mounted, the substrate was mounted via silver epoxy (to improve heat transfer) into a 1 x 1 x 0.105 inch nickel-gold plated, cold rolled steel package with 72 (18 to a side) glass-to-metal seal leads.

The chips were interconnected and the board connected to internal package leads by thermocompression bonding of a 0.001 inch diameter gold wire. After testing, the package was enclosed by a 0.012 inch thick nickel-gold plated, cold rolled steel cover.

Versatility

Typifying the variety of circuits that can be built on the basic board are these four different types of circuits.

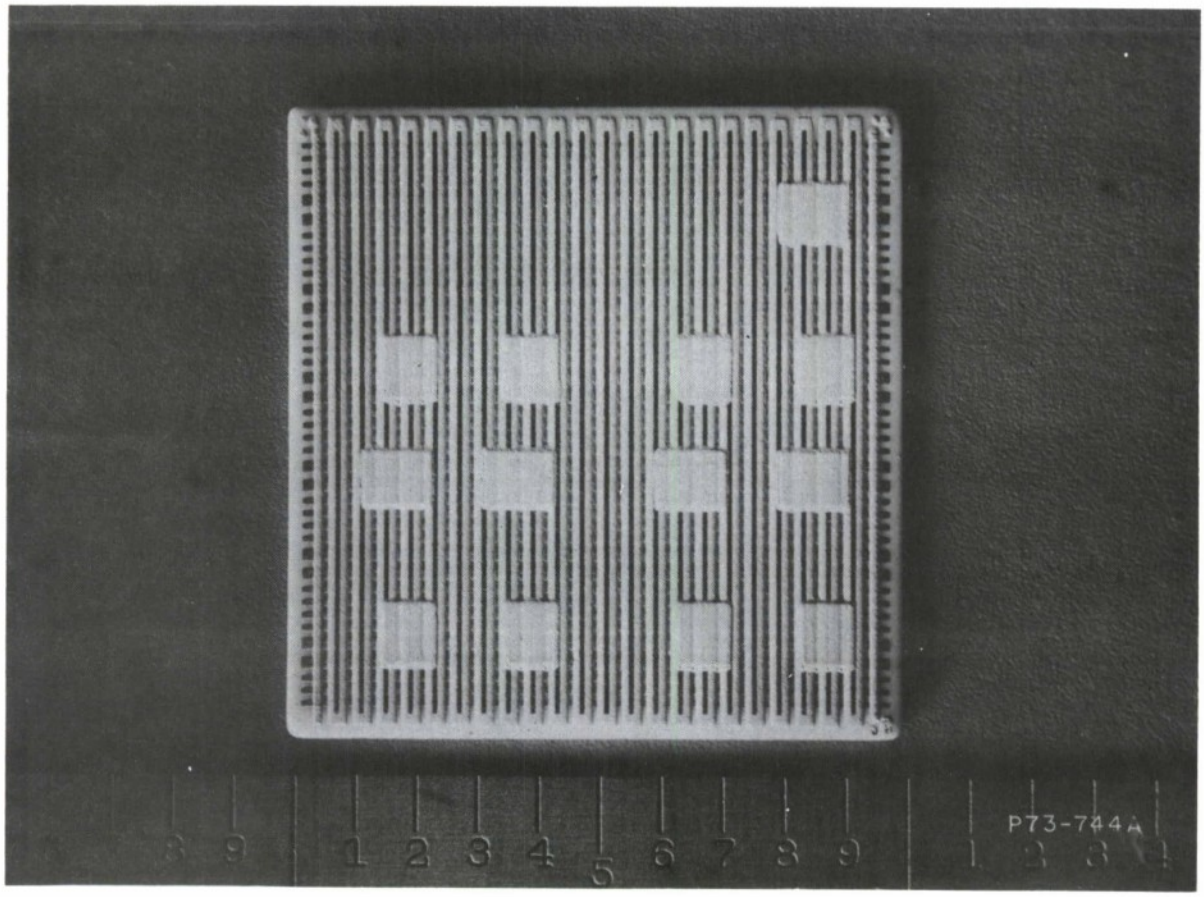

Fig. 6. Dielectric chip mounting pads.

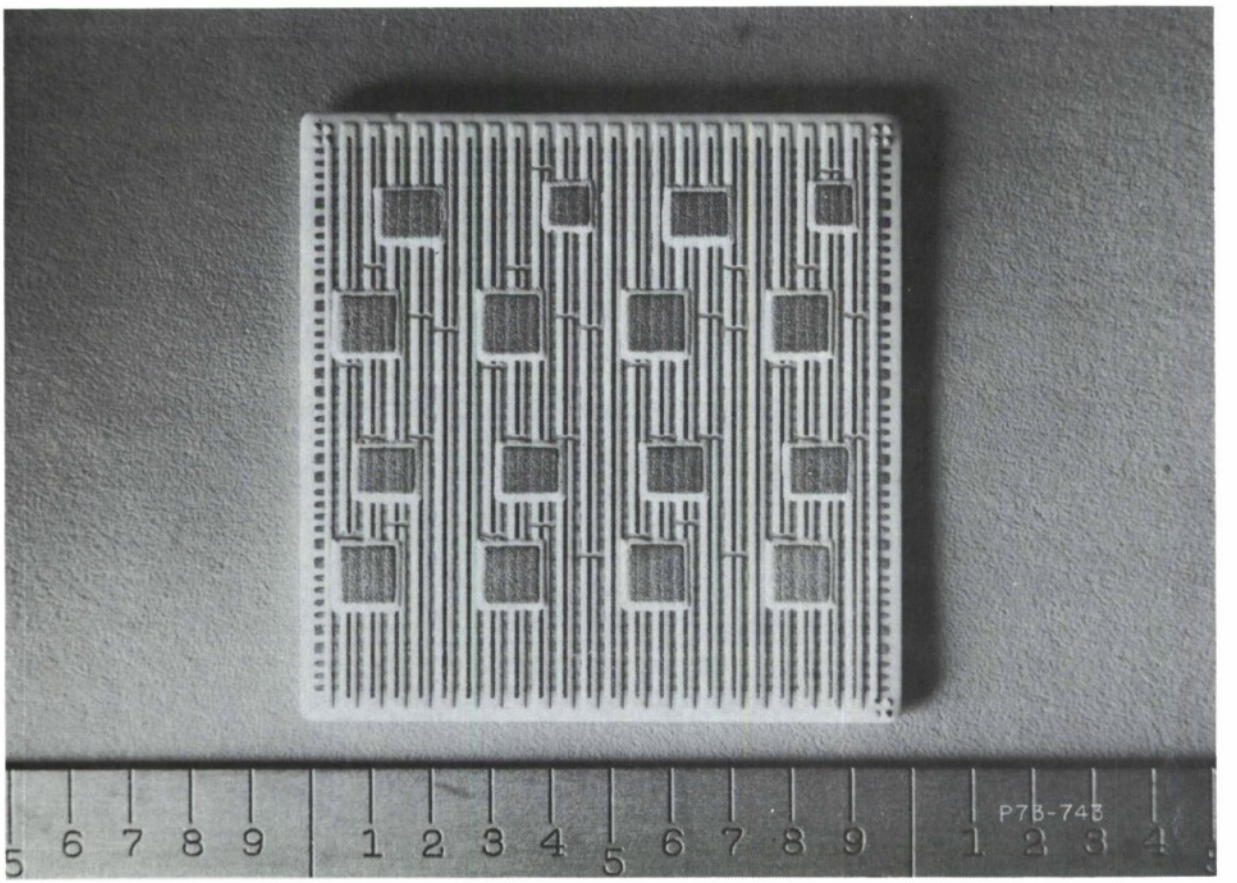

Fig. 7. Metalized dielectric chip mounting pads with cuts in top and bottom conductors for interconnecting purposes.

1. Fifteen TTL flip flops that comprise a 15-stage counter (Fig. 8) that can be used as a timing function for most digital memory and computer systems. In one of the first designs made at Lincoln Laboratory, connections to the bottom conductors were made via 0.010 inch openings, which were impractical to fabricate in large quantities. This led to the use of dielectric lines on future circuits.
2. A binary number multiplier (Fig. 9) that consists of five dual 2 wide input AND-OR invert gates, three quadruple 2 input NOR gates and one dual 4 input NAND buffer.
3. A digital filter (Fig. 10) used in a computer that consists of a 4-bit by 4-bit multiplier providing an 8-bit product. Devices featured are five quadruple 2-input NOR gates and eight 2-bit binary full adders.
4. An array multiplier of binary numbers (Fig. 11) without need for external timing and control that consists of two dual 4-input NAND buffers, six quadruple 2-input NOR gates and eight 2-bit binary full adders.

Conclusions

This thick film design offers these advantages to circuit designers.

1. Low cost fabrication.
2. High yield (Appendix A).
3. Fast turnaround.
4. Optimum breadboard.

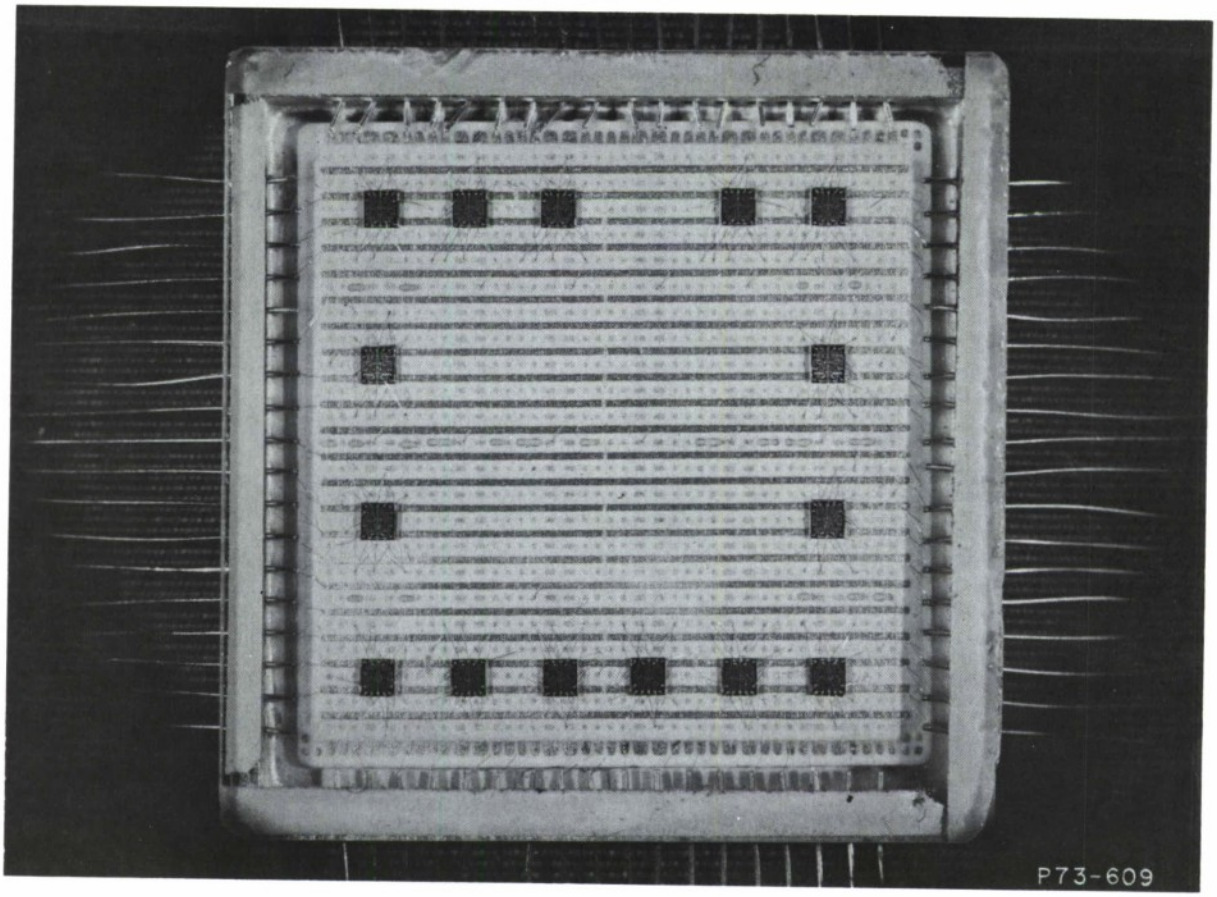

Fig. 8. Fifteen stage binary counter (preliminary design).

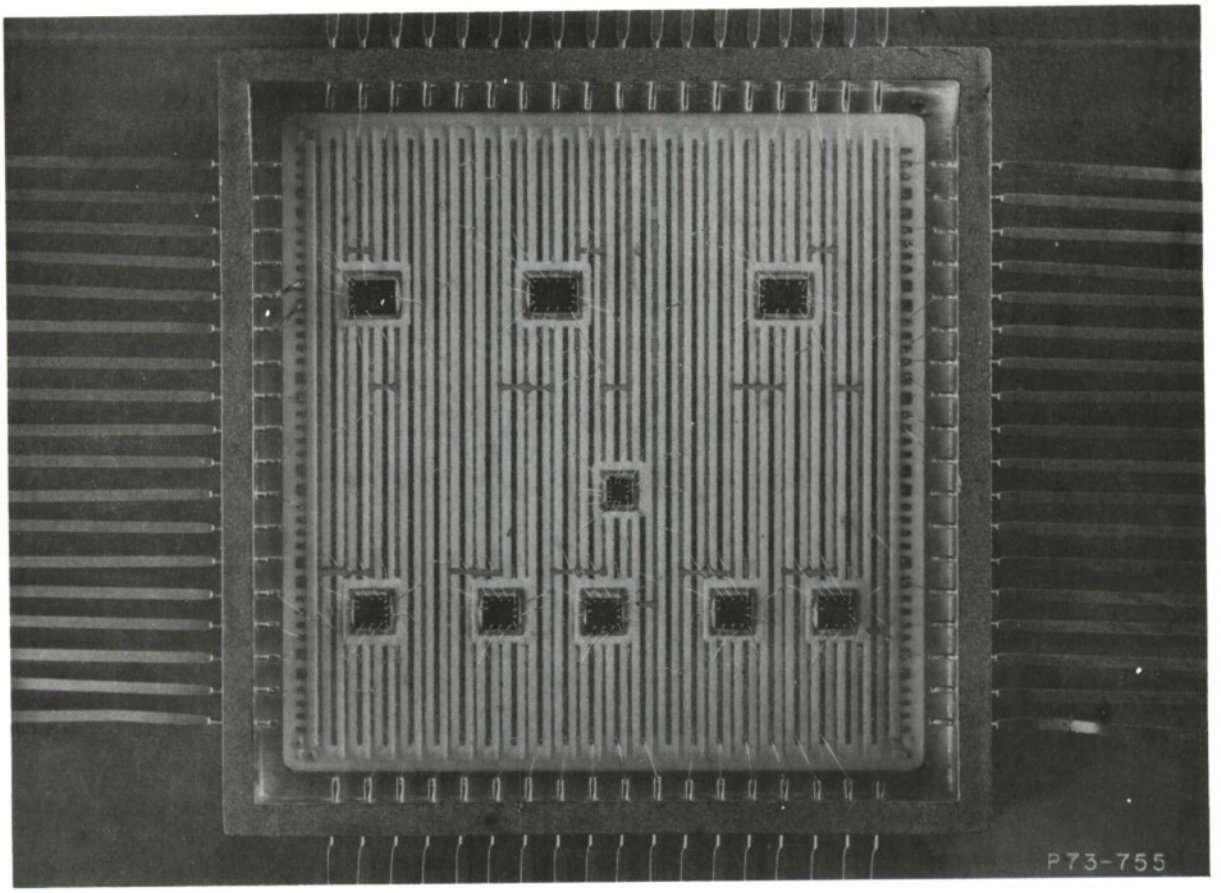

Fig. 9. Binary number multiplier.

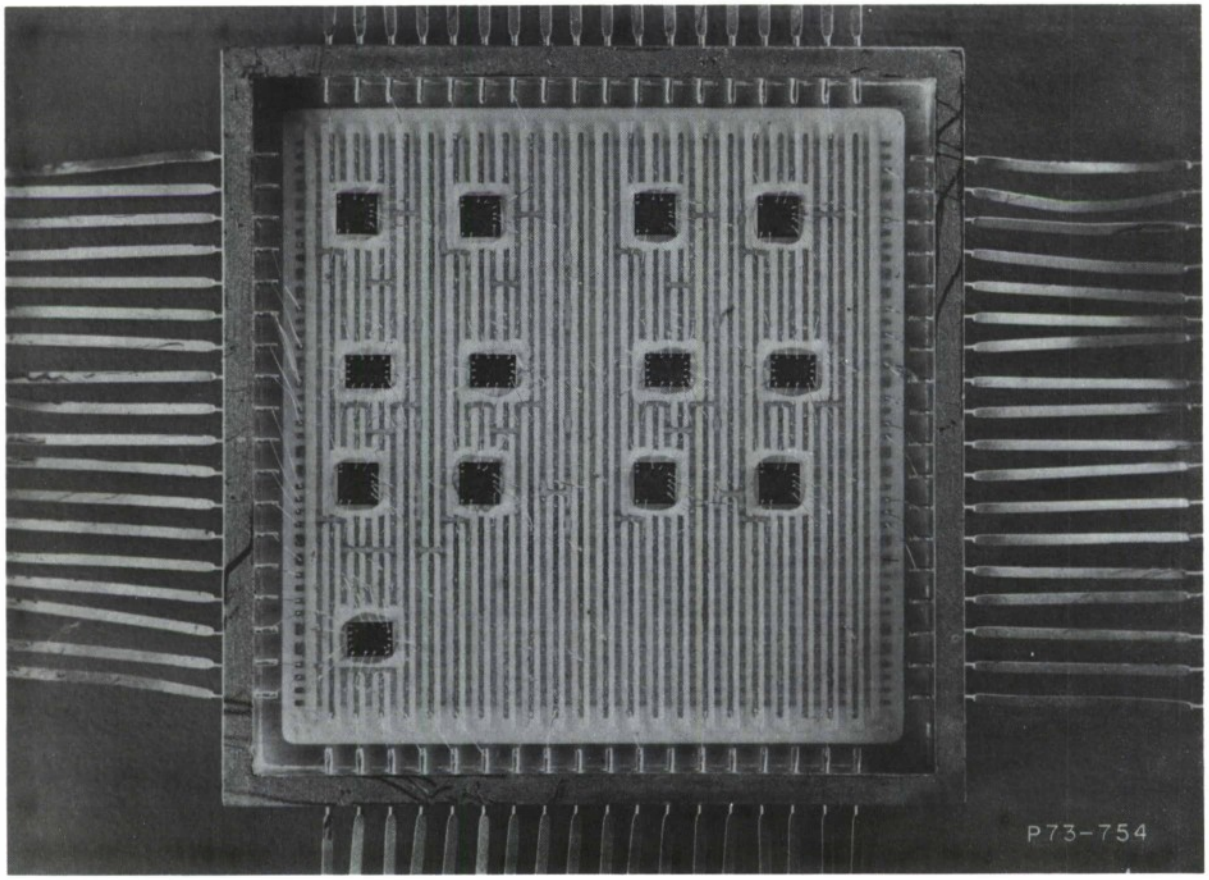

Fig. 10. Digital filter.

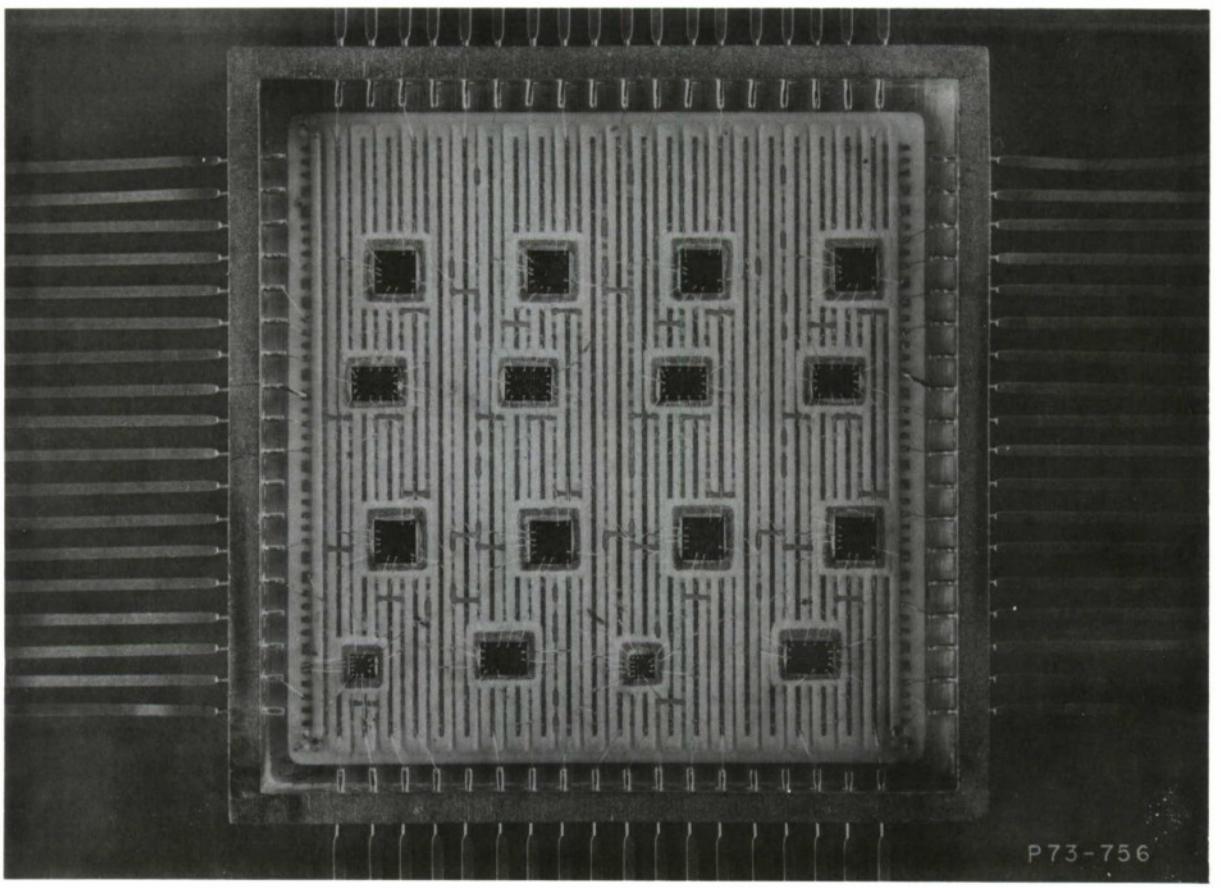

Fig. 11. Array multiplier.

There are also some disadvantages.

1. Limited chips per substrate.
2. Limited package leads.
3. Necessity of a heat sink for high power applications.

The fabrication method described is only one of several ways to produce the basic board. One of the other methods, Lincoln's standard multilayer interconnecting pattern (Fig. 12) makes use of a multilayer ceramic wiring structure on which the E. I. DuPont de Nemours & Company, Inc., has a patent pending, and which facilitates mass production of the boards.

Boards, even smaller than the one described, could be stacked and interconnected by risers to create a most compact microcircuit package (Fig. 13). Conductors could be screened on top of the riser and solving the problem of "around the edge" connections. The exposed riser surface could be used to interconnect, or as a pickup for an electron beam or other source which could activate various devices on the substrate surface.

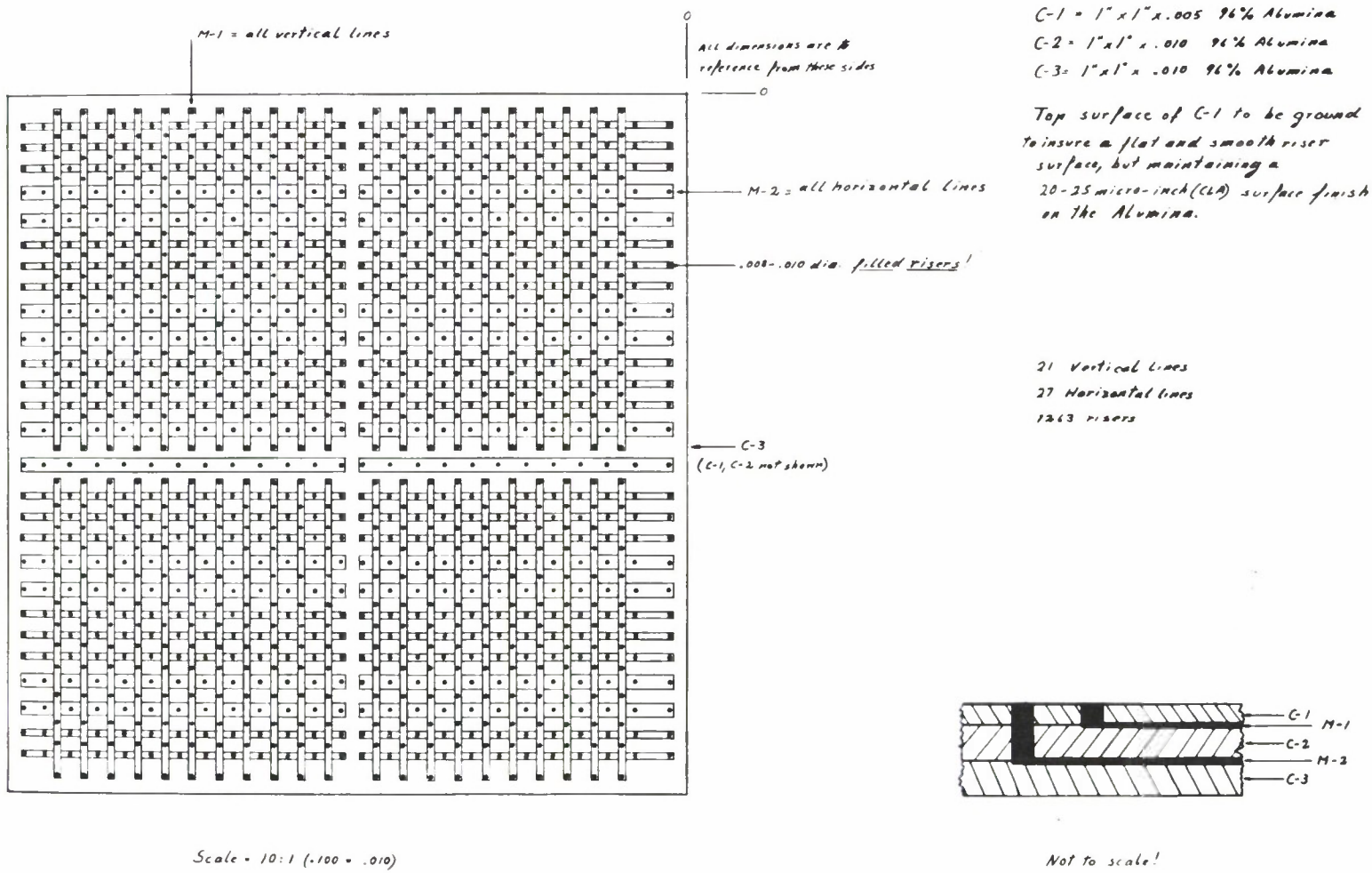

Fig. 12. Standard multilayer interconnecting pattern with buried metalization and risers.

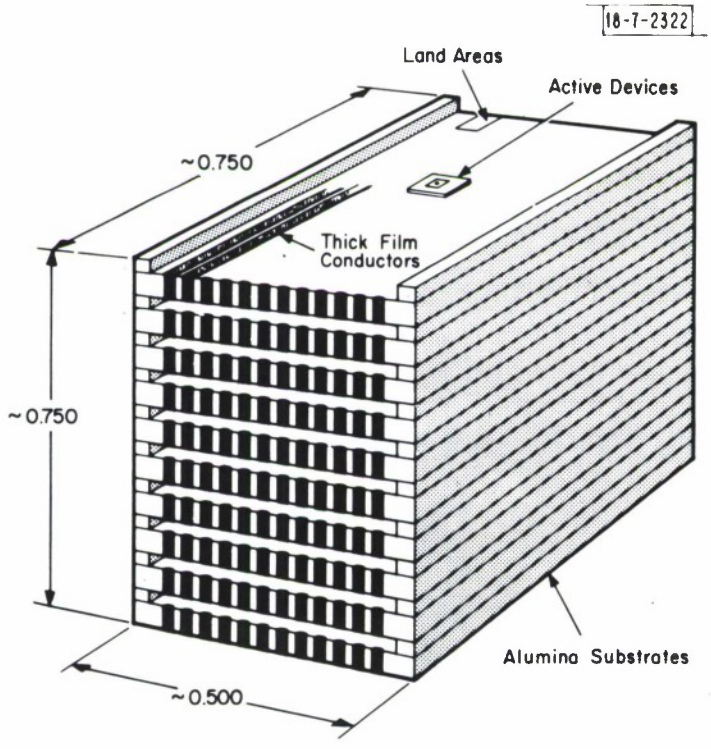

Fig. 13. Stacked dynode array.

Appendix A

Test Results

Substrates started: 300

Substrates lost: 60

Yield: 80 percent

Feasible yield: 92 percent if contamination problems are eliminated

Failure	Number Failed	Cause
Bottom conductor line breaks	15	Hairs or lint picked up during screening
Shorts between adjacent conductor lines	6	Spreading of conductor paste due to substrate surface defects
Bottom conductor line skips	7	Clogged screen
Cracked dielectric after firing	1	Possible stress
Pinholes in dielectric	3	Trapped air bubbles
Cracked substrate during firing	4	Stresses in alumina
Top conductor line breaks	10	Hairs or lint picked up during screening
Top conductor line skips	2	Clogged screen
Shorts* between top and bottom conductor lines	12	Dielectric pinholes

*156 shorts found in 221,364 crossovers - averaged 13 shorts per substrate.

Appendix B
Equipment

The major equipment used is commercially available. (In addition to the usual "self-leveling, constant squeegee pressure," the squeegee head on the printer can be lowered or raised from left to right and locked in place to facilitate screening of wedge-shaped ceramics for special applications.) The equipment used is:

1. Furnaces: BTU 4-zone, digit set, variable incline, quartz muffle, speed control with readout in inch/min. and nichrome V belt. Maximum operating temperature: 1100°C ± 2°C per controlled zone.
2. Screen printer: Presco basic Model 200 built to Lincoln Laboratory specifications. Six inch by six inch maximum substrate size; 8 x 10 in. maximum screen size.
3. Thickness measuring instrument: Carl-Zeiss light section microscope. 1-150 microns useful measuring range.
4. Screen exposure source: Preco. 4-1/4-inch diameter collimated ultraviolet exposure light.
5. Screen tension measurements: Presco Model STG-3 screen tension gauge.
6. Viscometer: Brookfield Model HAT with helipath stand and T spindles.
7. Stereo zoom microscopes.
8. Nikon profile projector Model 6C.
9. Thixothropic mixers.
10. Freas Model 605 stainless steel drying ovens.

11. Environmental test: Associated Testing Lab test camber Model RK-1100; -70 to +215°C range.

12. Electrical test equipment: Digital ohmmeter, millivolt meter, megohmmeter, digital capacity meter and associated hardware.

Appendix C

Substrates

The 1 x 1 x 0.025-inch, 96-percent Al_2O_3 substrates were purchased "as fired." As their normal maximum camber of 0.004/inch was considered excessive, the substrates were passed through a flatness gauge to eliminate those with a camber greater than 0.002/inch. Substrate thickness was also checked and held to within ±0.001-inch. Holding these tolerances meant better control of the screen-printed lines with less spreading.

Substrates that met the desired tolerances were cleaned ultrasonically in detergent and water, rinsed in hot demineralized water, and degreased in alcohol vapor. They were then baked in a forced air oven at 125°C for one hour, cooled and stored in clean plastic bags.

Appendix D

Screening Inks

Screening inks were selected on the basis of their metal-to-glass ratio, adhesion, bondability, refireability, and viscosities, which were measured at 72°F, 45-percent relative humidity with a Brookfield Model HAT viscometer, helipath stand and C type T-spindle at 5 rpm.

High viscosities were lowered by adding the manufacturer's prescribed thinner. Low viscosities were raised by baking the inks in a vacuum oven for certain time periods at 100°C. Measurements were taken after cooling the inks to 72°F and rolling them on a thixothropic mixer for a couple of hours. After the desired viscosities were obtained, the inks were stored on a slow rolling thixothropic mixer until ready for use.

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13. ABSTRACT

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14. KEY WORDS

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dielectrics